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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,196	05/18/2005	Hideya Kumoni	03500.017757	5637

5514 7590 04/26/2007
FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER

RAO, G NAGESH

ART UNIT	PAPER NUMBER
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1722

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/535,196

Applicant(s)

KUMONI, HIDEYA

Examiner

G. Nagesh Rao

Art Unit

1722

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-46 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-46 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 May 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. ____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____ |

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1) Claims 1-12, 31, and 44-46 are rejected under 35 U.S.C. 102(b) as being anticipated by Sugahara (US Patent No. 4,822,752).

Sugahara 752 pertains to the process for producing single crystal semiconductor layer and semiconductor device produced by said processes, whereby it is taught producing a crystalline thin film by melting and recrystallization in a specific region separate from a non-surrounding region having a locally melt and recrystallization process as shared with the non-surrounding region by a common boundary. Furthermore as taught by Sugahara 752 the processes steps set forth in the claimed language may be repeated resulting in crystallizing of areas to grow in the direction of shifting while ensuring that regions prepared for forming the crystalline thin film are aligned in an orderly fashion as each spot in a shifting forward manner is spot treated via a laser deposition to melt and recrystallize said section of the thin film as it is being created before proceeding to the next section.

Furthermore Sugahara 752 teaches A process for producing a crystalline thin film, wherein an area including a part of a boundary between a position-controlled crystal grain of a thin film and the surrounding region is made a melting-recrystallized area, and the crystal grain is made to laterally grow by a melting-recrystallization step in which the melting-recrystallized area is locally heated pulsewise, and molten and recrystallized.

Finally Sugahra 752 teaches an element formed by using the crystalline thin film obtained in the processing steps above, wherein a spatial position of at least a part of a crystal grain having a continuous crystal structure is determined by a spatial position of a specific region in a starting thin film, and a crystal grain having the controlled spatial position is used in an active region, whereby the active region is formed in a single crystal grain of the crystalline thin film, forming in end a circuit comprising a plurality of elements which are connected to one another by a wire (See Abstract, Figs 1-17B, Col 1 Lines 9-51, Col 3 Lines 54-68, Col 4 Lines 1-68, Cols. 7-9, 11, 13, and 15 Lines 1-68).

2) Claims 13-43 are rejected under 35 U.S.C. 102(b) as being anticipated by Jung (US Patent No. 6,346,462).

Jung 462 pertains to the method of fabricating a thin film transistor, whereby it is taught via sequential lateral solidification a process for fabricating thin film crystalline materials via focusing an array of energy in a particular region and melting said region in efforts to shift after the localization in order to have a desired growth of crystal grains to form after said processing.

Furthermore Jung 462 teaches a process for producing a crystalline thin film, wherein an area including a part of a boundary between a position-controlled crystal grain of a thin film and the surrounding region is made a melting-recrystallized area, and the crystal grain is made to laterally grow by a melting-recrystallization step in which the melting-recrystallization area is locally heated pulsewise, and molten and recrystallized.

Finally of which Jung 462 teaches The process for producing a crystalline thin film whereby, the position-controlled crystal grain is a single crystal grain provided in the specific region of a precursor of the thin film and wherein the precursor of the thin film is an amorphous thin film, and the single crystal grain provided in the specific region is a crystal grain grown

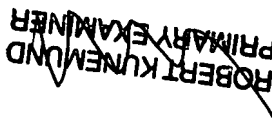
by solid phase crystallization of the amorphous thin film (See Figs 4A-4D, Cols 1-5 Lines 1-68).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to G. Nagesh Rao whose telephone number is (571) 272-2946. The examiner can normally be reached on 9AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yogendra Gupta can be reached on (571)272-1316. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


ROBERT KUNEMUND
PRIMARY EXAMINER


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GNR